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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,717	03/04/2002	Shigeru Nakamura	H-1034	2183

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MATTINGLY, STANGER & MALUR, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER

ZARNEKE, DAVID A

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 11/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,717	NAKAMURA ET AL. <i>nee</i>	
	Examiner	Art Unit	
	David A. Zarneke	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 and 19-43 is/are pending in the application.
- 4a) Of the above claim(s) 1-7 and 21-43 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 8-17, 19, 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 8/18/03 have been fully considered but they are not persuasive.

Applicant argues that the secondary reference Takiar fails to teach "pressure welding" of a flip chip as claimed in the present invention.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner asserts that the applicant has attacked the individual references as opposed to considering the rejection as a whole. The rejection relies on Figures 3 and/or 4 of Hiroyuki to teach the flip chip bonding of a first chip to a substrate, attaching a second chip to the first chip and then the wire bonding of a second chip to the substrate. Then Takiar is combined with Hiroyuki to teach (1) the application of pressure to the first chip so as to electrically connect it to the electrodes of the wiring substrate and (2) the pressure applied to the second chip being smaller than the pressure applied to the first chip.

Takiar teaches the soft solder bonding of the first chip to the wiring substrate and therefore is relevant to the flip chip bonding of the present invention even though the

figures show the solder is applied to the entire interface between the first chip and the substrate. Regardless of this difference, the concept of controlling the application of pressure would apply to both inventions because they both use solder.

Further, the fact that Takiar teaches wire bonding the first chip to the substrate is a piecemeal attack on the references used in the rejection as opposed to considering the rejection as a whole.

Hiroyuki is relied upon to teach the flip chip bonding of the first chip and Takiar is relied upon to teach the application of and control over pressure used to bond the chips. The fact that Takiar wire bonds the first chip is not relevant because the reason for using Takiar is its teaching that pressure is used to solder bond the first chip to the substrate and a lower pressure is used to adhesively attach the second chip to the first chip.

Therefore, the rejections presented in the previous office actions stand as written. In order to be complete, these rejections will be re-stated below.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 8, 14, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al., JP 2000188369, in view of Takiar et al., US Patent 5,422,435.

Hiroyuki teaches a device comprising:

(a) preparing a wiring substrate (4) having a plurality of electrodes (6) created on a main surface thereof;

(b) preparing a first semiconductor chip (1a) having a main surface, a back surface, a plurality of semiconductor devices created on said main surface of said first semiconductor chip and a plurality of electrodes created on said main surface of said first semiconductor chip;

(c) preparing a second semiconductor chip (1b) having a main surface, a back surface, a plurality of semiconductor devices created on said main surface of said second semiconductor chip and a plurality of electrodes created on said main surface of said second semiconductor chip and having a thickness smaller than a thickness of said first semiconductor;

(d) placing said first semiconductor chip on said main surface of said wiring substrate with said main surface of said first semiconductor chip interfacing with said main surface of said wiring substrate in such a way that said electrodes provided on said main surface of said first semiconductor chip interface with said respective electrodes provided on said main surface of said wiring substrate;

(e) electrically connecting said electrodes created on said second semiconductor chip to said respective electrodes provided on said wiring substrate by using a plurality of wires; and

(f) forming a resin sealing body (5) for sealing said first semiconductor chip, said second semiconductor chip and said wires (Figures 4 & 5).

Hiroyuki fails to teach (1) the application of pressure to 1st chip so as to electrically connect it to the electrodes of wiring substrate and (2) the pressure applied to the 2nd chip being smaller than the pressure applied to the 1st chip.

Takiar teaches a stacked multi-chip module (figure 5) comprising providing a carrier member (152), such as a lead frame (5, 26+), or a substrate having leads thereon (8, 25+), on which a 1st chip (146) is pressure adhered, a 2nd chip (148) pressure adhered to the 1st chip using a pressure smaller than the pressure used to apply the 1st chip (10 34+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the pressure bonding of Takiar as the method of bonding the chips in the invention of Hiroyuki because pressure bonding is a conventionally known in the art method of bonding chips or substrates.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Regarding claim 14, Hiroyuki teaches applying solder balls (6) to the back side of the wiring substrate (Figures).

With respect to claims 15 and 16, Takiar teaches applying a 3rd chip to the substrate and a 4th chip on top of the 3rd chip (Figure 10).

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al., JP 2000188369 in view of Takiar et al., US Patent 5,422,435 as applied to claim 8 above, and further in view of Lau, Flip Chip Technologies 1996, McGraw-Hill, p. 302-303.

Hiroyuki and Takiar both fail to teach the use of heat along with pressure to bond chips and or substrates together.

Regarding claim 9, the application of heat along with pressure is a conventionally known in the art combination known to be used in the bonding of chips (Lau).

With respect to claim 10, Lau teaches that the application of heat cures the resin thereby fixing the chip to the substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to the heat and pressure combination of Lau in the invention of Hiroyuki and Takiar because it is a conventionally known method of bonding chips to substrate.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claims 11, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al., JP 2000188369, in view of Takiar et al., US Patent 5,422,435, as applied to claim 8 above, and further in view of Okazaki et al., US Patent 6,269,999.

Both Hiroyuki and Takiar fail to teach the use of ultrasonic/supersonic waves in the bonding of solder balls attached a chip to a substrate.

Okazaki teaches chip mounting using ultrasonic vibrations to bond a chip having balls mounted on its electrodes (abstract & Figures).

It would have been obvious to one of ordinary skill in the art at the time of the invention to the ultrasonic bonding of Okazaki in the invention of Hiroyuki and Takiar because it is a conventionally known method of bonding chips to substrates (1, 21+).

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al., JP 2000188369.

Hiroyuki teaches a device comprising:

(a) preparing a transfer mold (abstract) which is inherently provided with a cavity having first and second side surfaces facing each other and third and fourth surfaces facing each other and coming in contact with said first and second side surfaces;

(b) preparing a wiring substrate (3) having a main surface, preparing a first semiconductor chip (1a) fixed on said main surface of said wiring substrate and preparing a second semiconductor chip (1b) fixed on said first semiconductor chip;

(c) inherently placing said wiring substrate, said first semiconductor chip and said second semiconductor chip inside said cavity; and

(d) after said step (c), injecting resin through said resin injection entrance in order to seal and hold said first and second semiconductor chips, wherein in said step (c), said wiring substrate, said first semiconductor chip and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said third side surface of said cavity, the length of said first semiconductor chip exceeds the length of said second semiconductor chip;

wherein in said step (c), said wiring substrate, said first semiconductor chips, and said second semiconductor chips are arranged in such a way that, on a cross section parallel to said first side surface of said cavity, the length of each of said first

semiconductor chips are smaller than the length of corresponding second semiconductor chips stacked on said first semiconductor chips. (figures).

While Hiroyuki fails to teach the mold to be provided with a resin injection entrance created on said first side surface, the positioning of a resin injection entrance is an obvious matter of design choice.

Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(a)).

Regarding claim 19, the use of an air hole in the cavity is conventionally known in the art.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al., JP 2000188369, in view of Mitsuhiro, JP 03-106622.

Hiroyuki teaches a device comprising:

(a) preparing a transfer mold (abstract) which is inherently provided with a cavity having first and second side surfaces facing each other and third and fourth surfaces facing each other and coming in contact with said first and second side surfaces;

(b) preparing a wiring substrate (3) having a main surface, preparing a first semiconductor chip (1a) fixed on said main surface of said wiring substrate and preparing a second semiconductor chip (1b) fixed on said first semiconductor chip;

(c) inherently placing said wiring substrate, said first semiconductor chip and said second semiconductor chip inside said cavity; and

(d) after said step (c) injecting resin through said resin injection entrance in order to seal and hold said first and second semiconductor chips, wherein in said step (c), said wiring substrate, said first semiconductor chip and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said third side surface of said cavity, the length of said first semiconductor chip exceeds the length of said second semiconductor chip,

wherein in said step (c), said wiring substrate, said first semiconductor chips, and said second semiconductor chips are arranged in such a way that, on a cross section parallel to said first side surface of said cavity, the length of each of said first semiconductor chips are smaller than the length of corresponding second semiconductor chips stacked on said first semiconductor chips. (figures).

While Hiroyuki fails to teach the mold to be provided with a resin injection entrance created on said first side surface, the positioning of a resin injection entrance is an obvious matter of design choice.

Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(a)).

Also, while Hiroyuki fails to teach the use of a plurality of device areas on the substrate, a plurality of 1st chips and a plurality of 2nd chips, it would have been obvious to one of ordinary skill in the art to make a strip lead frame-type of wiring substrate where multiple individual chip stacks can be formed thereon.

The mere duplication of parts has no patentable significance unless a new and unexpected result is produced. In re Harza, 124 USPQ 378 (CCPA 1960).

Finally, Hiroyuki also fails to teach the use of a plurality of resin injection entrances.

Mitsuhiro teaches a semiconductor molding process wherein a resin is flowed into a cavity containing a semiconductor package wherein there exist 2 entrance gates (3), both on the same side of the cavity.

It would have been obvious to one of ordinary skill in the art to use the multiple resin entrance gates of Mitsuhiro in the transfer molding of Hiroyuki because Mitsuhiro teaches that heat can be absorbed effectively, pressure can be easily applied and the molding cycle time can be improved.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Application/Control Number: 10/086,717
Art Unit: 2827

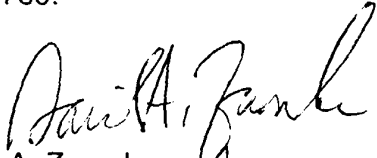
Page 11


The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 5,696,031, US Patent Application Publication 2002/0045290, JP 405013662, JP 63-179537, and JP 63-104343 are all cited as teaching inventions very similar to the present invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-F 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703)-308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-6789.


David A. Zarneke
October 10, 2003


EVAN PERT
PRIMARY EXAMINER